APPLICATION DATA SHEET

APPLICATION INFORMATION

Filing Date::	03/17/04
Application Type::	Regular
Subject Matter::	Utility
Title::	Circuits and Methods for Analyzing Timing Characteristics of Sequential Logic Elements
Attorney Docket Number::	X-1039-1D US
Request for Early Pub?::	No
Request for Non-Pub?::	Yes
Total Drawing Sheets::	6
Small Entity?::	No
Petition included?::	No

APPLICANT INFORMATION

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	Germany
Status::	Full Capacity
Given Name::	Peter
Middle Name::	H.
Family Name::	Alfke
Street::	25251 La Rena Lane
City::	Los Altos Hills
State or Province::	CA
Postal or Zip Code::	94022

Applicant Authority Type::	Inventor
Primary Citizenship Ctry::	India
Status::	Full Capacity
Given Name::	Himanshu
Middle Name::	J.
Family Name::	Verma
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City:: Mountain View
State or Province:: CA
Postal or Zip Code:: 94041

CORRESPONDENCE INFORMATION

Correspondence Customer Number:: 24309

REPRESENTATIVE INFORMATION

Representative Customer Number::	**24309**	

DOMESTIC PRIORITY INFORMATION

Application::	**Continuity Type::**	**Parent Application::**	**Parent Filing Date::**
This Applic.	Divisional	10/198,801	July 19, 2002

ASSIGNEE INFORMATION

Assignee Name:: Xilinx, Inc.
Street:: 2100 Logic Drive
City:: San Jose
State or Province:: California
Postal or Zip Code:: 95124